



# Welcome To The RISC-V Revolution!



**Daejeon, Korea**

June 17<sup>th</sup>, 2019



Feb 2019 USA || Mar & May 2019 China || May 2019 Europe || Jun 2019 Asia-Pacific || Jun 2019 Australia  
Jun 2019 China || Jul 2019 Pakistan || Aug 2019 India || Aug 2019 USA || Sep 2019 Middle East || Oct 2019 China  
Nov 2019 Mexico || Nov 2019 South America

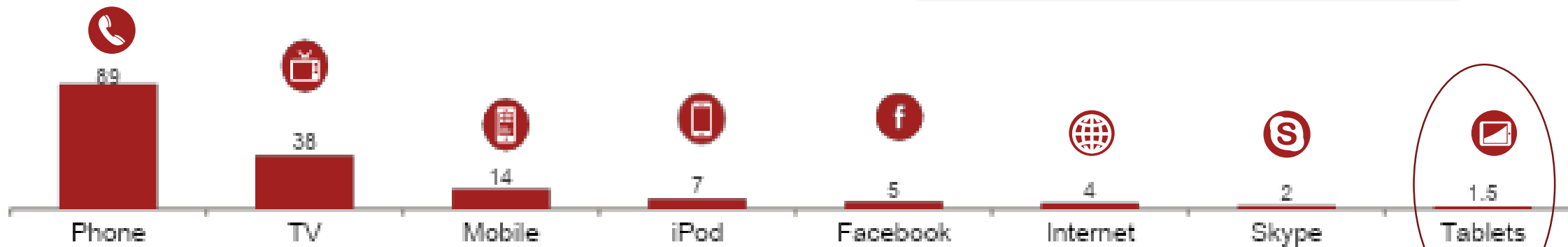
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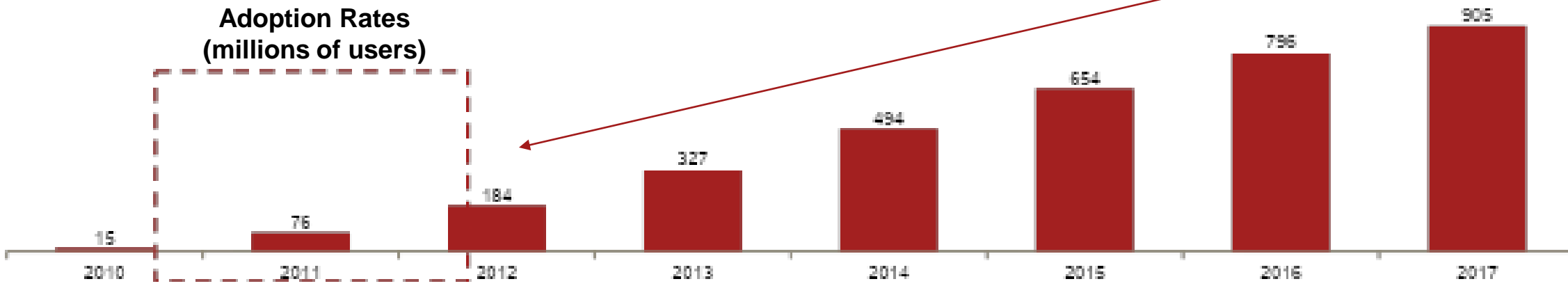
# New Multi-Billion-Dollar Markets are Being Created in Quarters, Not Decades

## Number of Years to reach 150 million total users

Fast Time to Market is a Competitive Advantage for Modern SOC Companies



## Tablet/eReader Adoption Rates (millions of users)





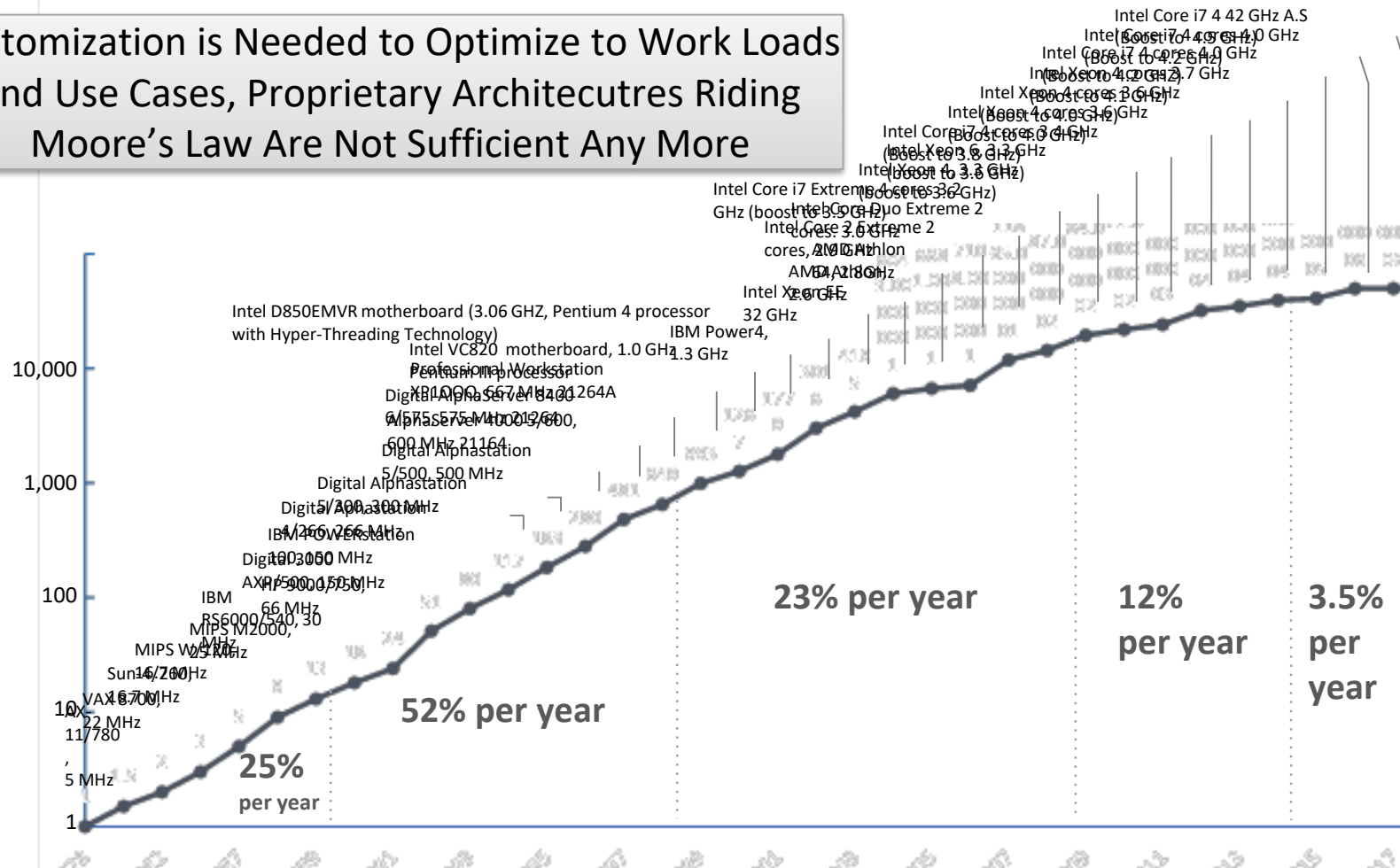
# The Benefits of Moore's Law are Slowing; Moore's Law is Financially Failing

## Moore's Law Has Stalled

## Time for a Paradigm Shift

General-purpose CPU performance (vs. VAX-11/780)

Customization is Needed to Optimize to Work Loads and Use Cases, Proprietary Architectures Riding Moore's Law Are Not Sufficient Any More



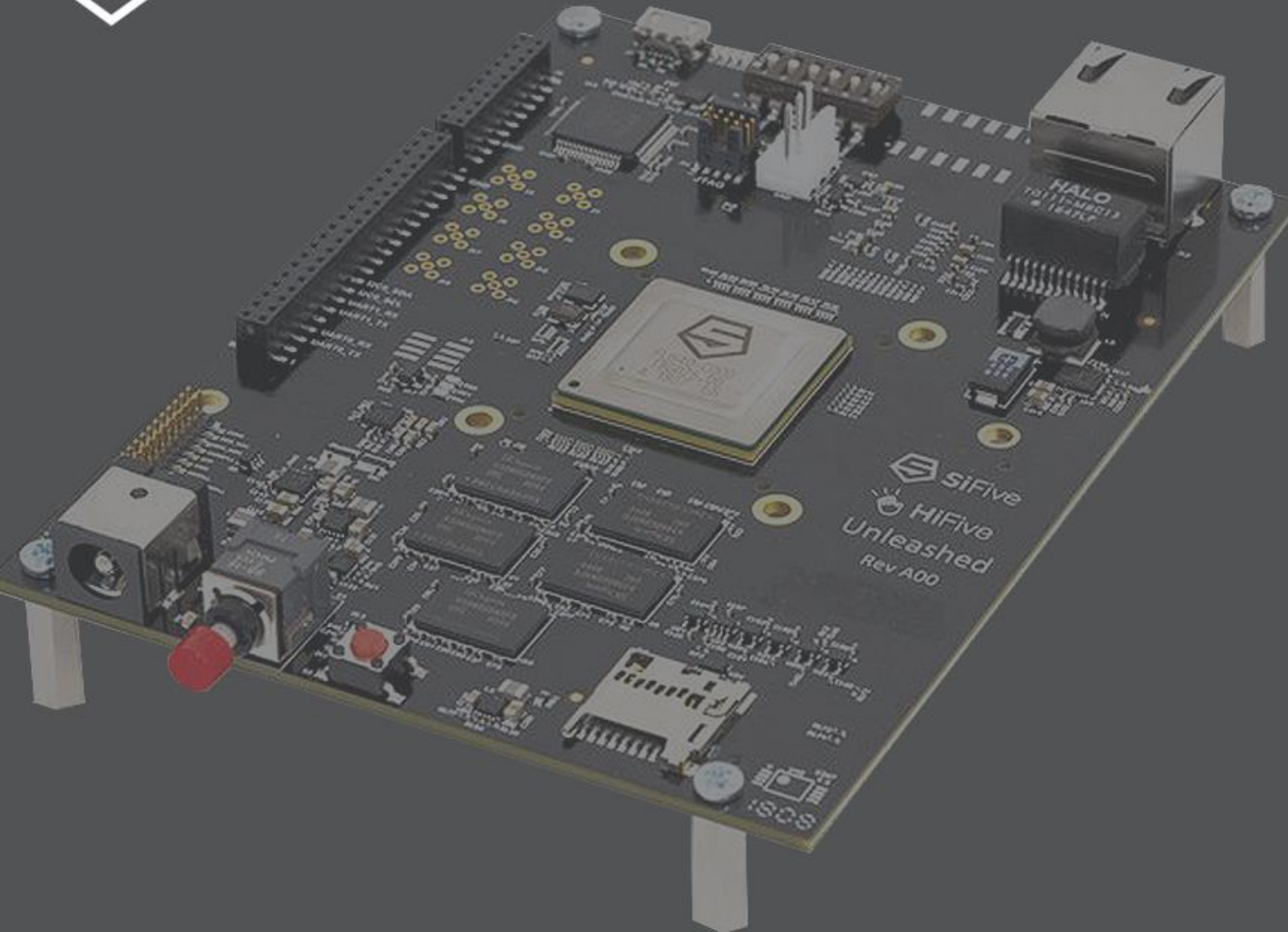
**Customization** is the only way to get performance

**One-Chip-Fits-All no longer applies**

**Innovation** is desperately needed to meet the needs of new applications running on billions of devices

Source: Hennessy, Patterson, Computer Architecture 6e  
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Time	Agenda
09:30 - 09:40	Welcome and Introduction, by Brandon Cho, SiFive
09:40 - 10:10	RISC-V History and State of the Union, by Yunsup Lee, Co-Founder and CTO, SiFive
10:10 - 10:30	<b>Keynote:</b> Leading Semiconductor Design Revolution, by Keith Witek, SVP Corporate Development and Strategy, SiFive
10:30 - 10:50	SW Requirements for Flexible Memory Alignments, Samsung
10:50 - 11:00	Break
11:00 - 11:20	Furiosa NPU: High Performance AI Inference Chip for Datacenter and Enterprise, FuriosaAI
11:20 - 11:40	Freedom HiFive RISC-V Development Platforms, by David Lee, Product Manager, SiFive
11:40 - 12:00	Heterogeneous Analytics and Debug of RISC-V and ARM Based SoC, UltraSOC
12:00 - 13:00	Lunch and Demos
13:00 - 13:20	RISC-V Core IP for Target Vertical Markets, by Yunsup Lee, Co-Founder and CTO, SiFive
13:20 - 13:40	DesignShare: Reducing Prototype IP Costs to Zero, OpenEdges
13:40 - 14:00	RISC-V Core Software Ecosystem, by Yunsup Lee, Co-Founder and CTO, SiFive
14:00 - 14:20	Professional Development Tools for RISC-V, IAR Systems
14:20 - 14:30	Break
14:30 - 15:00	University Programs, by Jeff Mulhausen, Chief Evangelist, SiFive
15:00 - 15:20	University Platform and Hackathon Program, by David Lee, Product Manager, SiFive
15:20 - 15:30	Break
15:30 - 16:00	<b>Tutorial:</b> SiFive Core Designer, David Lee, Product Manager, SiFive
16:00 - 16:10	Video: Design Your Own CPU!
16:10 - 16:20	Closing Remarks, by Brandon Cho, CEO, SiFive Korea
16:20 - 17:00	Networking and Demos



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The most advanced configurable core IP and silicon solutions from the inventors of RISC-V.

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